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Applicant:	:	**Hofstee, et. al.**	
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Group Art Unit:	:	**2182**	
Examiner:	:	**Hassan, Aurangzeb**	
Docket No.	:	**AUS920030403US1**	
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/ Joseph T. Van Leeuwen, Reg. No. 44,383/	3/9/2007
Joseph T. Van Leeuwen, Reg. No. 44,383	Date

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

In response to the Final Office Action having a mailing date of December 15, 2006, Applicants respectfully request review of the rejections to the claims in the above-identified application. No amendments are being filed with this request. This request is being filed with a notice of appeal. The review is requested for the reasons stated below. The fee for the Notice of Appeal is submitted herewith. No extensions of time or other fees are believed to be necessary. If, however, an extension fee or other fee is required, the undersigned requests such extension, if applicable, and hereby authorizes the Commissioner to charge any such fees to Van Leeuwen & Van Leeuwen, Deposit Account No. 50-3754.

Status of the Claims and Prosecution History

Claims 8-27 are currently present in the Application, and claims 8, 15, and 21 are independent claims. Claims 8-27 stand finally rejected under 35 U.S.C. § 103 as allegedly

being obvious, and therefore unpatentable, over U.S. Patent No. 6,366,109 to Matsushita (hereinafter "Matsushita") in view of U.S. Patent No. 4,292,668 to Miller et al. (hereinafter "Miller"). In the first Office Action (mailed 12/30/05), claims 8-27 were rejected under § 102 as being anticipated by Matsushita. Applicants overcame the rejection in their Response dated 3/30/06 without amending any of the claims. In the second Office Action (mailed 7/5/06), claims 8-27 were rejected under § 103 as being obvious over Matsushita in view of Miller. In Applicants Response, dated 10/5/06, Applicants traversed the rejection without amending any of the claims. In the Final Office Action (mailed 12/15/06), the Examiner maintained, and made final, the rejections set forth in the second Office Action.

The Currently Cited Prior Art Does Not Support A Rejection Under 35 U.S.C. § 103

In the Final Office Action, the Examiner lists six arguments made by Applicants in refuting the rejection of Applicants' claimed invention. Applicants disagree with the Examiner's Response to Arguments set forth in the Final Office Action and respond as follows:

Argument 1 – Date of Miller reference is over a quarter century old. This is not really an argument of Applicants but rather an observation. The age of Miller also buttresses Applicants' argument that the type of interface controller being taught by Miller is fundamentally different from the interface controller being taught and claimed by Applicants.

Argument 2 – Other than teaching more than one interface controller, Miller does not teach or suggest any of the other claimed limitations. In the Examiner's response to Applicants' argument, the Examiner states that Matsushita "already teaches a plurality of I/O devices however does not explicitly mention the fact ... that an interface controller is present." This is a major problem with the Examiner's rejection. Most of the claim limitations are rejected as being taught by Matsushita. The primary focus of Applicants' claimed invention is to a "configurable interface controller." Applicants' title is a "System and Method for a Configurable Interface Controller," In Applicants' independent claims, interface pins are dynamically assigned by (1) receiving an assignment request, (2) identifying interface pins that correspond to the request, (3) selecting an interface controller from a plurality of interface controller that corresponds to the assignment request, and then (4) associating the identified interface pins with the selected interface controller. However, here the Examiner freely admits that the primary reference does not even mention that an interface controller is even present.

Applicants point in this Argument 2 is that Matsushita is focused on a semiconductor testing device and, as the Examiner admits, does not teach or suggest anything about interface controllers. Miller, on the other hand, does teach multiple DMA interface controllers (older controllers that used to be used for handling slow speed data), however Miller's 1981 patent does not teach selecting the interface controller in any fashion at all similar to that taught and claimed by Applicants. Miller does not teach receiving an assignment request, Miller does not teach identifying pins that correspond to the request, or selecting an interface controller that corresponds to the assignment request.

The Examiner's remarks to Applicants' arguments brings forth another argument of Applicants, namely, that there is no motivation to combine the teachings of Matsushita with those of Miller. The Examiner admits that Matsushita does not even mention the use of interface controllers to control I/O devices, while Miller teaches a way of sending work to slow DMA IOCs. There is no motivation to combine the references because, as the Examiner admits, Matsushita does not mention interface controllers so there is no motivation to combine the teachings of Matsushita with those of Miller as they are directed at entirely different problems and technologies. Matsushita is focused on semiconductor testing while Miller is focused on blocks of data to a particular type of interface controller. Applicants further contend that impermissible hindsight was used in rejecting Applicants' claims in view of Matsushita and Miller. No one would select these references unless they had the benefit of Applicants' disclosure.

Argument 3 – Matsushita does not teach the limitation of selecting an interface controller. The Examiner disagrees with this argument even though the Examiner admitted in the prior argument (Argument 2) that Matsushita does not even mention an interface controller. The Examiner points out that Matsushita's multiplexers (104, 106, and 108) are no longer being cited as teaching how the interface controllers are selected. However, as pointed out above, Miller does not teach any of the selection techniques that are taught and claimed by Applicants. While Miller selects an interface controller from a plurality of controllers, Miller's selection is not based on an assignment request, where the assignment request is also used to identify interface pins.

Argument 4 – Matsushita does not teach associating identified pins with the selected interface controller. Here the Examiner directs Applicant to figures 3 to 5 of Matsushita. However, as the Examiner already pointed out, Matsushita does not mention an interface

controller. Instead, figures 3 to 5 of Matsushita are directed to a "recognition decoder" that is simply not analogous or interchangeable with Applicants' interface controller. Matsushita teaches that the "recognition decoder" is found within pin assignment converter (90) and that the recognition decoder is used to activate a control bit that is fed to a group of multiplexers in the pin assignment converter when performing semiconductor testing (see, Fig. 4 of Matsushita and col. 6, lines 9-36). The Examiner contends that "The recognition decoder assists in the means of assigning pins (logical) with the connected I/O device (physical) via interface controller as explained in column 5, lines 65-67 and column 6, lines 1-44." What Matsushita is teaching is a way of testing different semiconductor packages where the logical pin assignments to the semiconductor package remain fixed, while the physical pin numbers differ for each semiconductor package. While Matsushita's semiconductor tester re-routes logical pins to different physical pins, it does not select an interface controller from a plurality of interface controller. In fact, Matsushita does not teach or suggest selecting any type of controller, instead it maps logical semiconductor pins to physical pin assignments in order to facilitate testing of different types of semiconductor packages. On the other hand, Miller teaches a plurality of interface controllers but does not teach selecting them based on an assignment request that also is used to identify the interface pins.

Argument 5 – In second Office Action, the Examiner no longer contends that Matsushita's "recognition controller" analogous to Applicants' interface controller. Applicant and the Examiner deal with the role of the recognition decoder in Argument 4 (para. no. 14 of Final Office Action and previous section of the paper).

Argument 6 – Examiner admits that Matsushita does not teach selecting a first interface controller from the assignment request and the Office Action added Miller for teaching plurality of interface controller, but the combination still does not render Applicants' claimed invention obvious. The Examiner states that Matsushita teaches "a testing system in which pin assignment is utilized in a number variety (sic) of I/O devices." The Examiner admits that Matsushita does not mention an interface controller is needed to connect the I/O devices. The Examiner attempts to equate the "semiconductors" that are being tested by Matsushita's device with I/O devices that would be connected to the interface controller taught and claimed by Applicants. Matsushita does not mention an I/O controller because an I/O controller is simply not used or needed to connect to the semiconductor packages that are being tested. Instead, Matsushita teaches using a semiconductor testing device 72 that is not equivalent to or

interchangeable with an interface controller. Also, Matsushita teaches a single semiconductor testing device and does not teach or suggest any method of selecting the semiconductor testing device from a plurality of testing devices, in contrast to Applicants' claimed invention that teaches and claims selecting an interface controller from a plurality of interface controllers.

The Examiner conclude (para. no. 16) by stating that "one of ordinary skill in the art would recognize that Miller's teaching of how a device is connected to a system would be utilized in Matsushita's system of connected devices." Applicants respectfully disagree. As pointed out above, Miller and Matsushita are directed at two entirely different technologies. Miller is directed at multiple interface controllers and had nothing to do with semiconductor testing. Miller does not teach or suggest selecting an interface controller by receiving an assignment request, identifying pins that correspond to the request, selecting one of the controllers that corresponds to the assignment request, or associating the identified pins with the selected interface controller. Matsushita, on the other hand, teaches a way of mapping logical pins to physical semiconductor pins in order to facilitate testing of a semiconductor package but is not concerned with interface controllers and, in fact, as pointed out by the Examiner, does not even *mention* interface controllers. Therefore, no motivation to combine the references plausibly exists in the references themselves. Instead, one would only be motivated to combine the references after having benefit of Applicants' disclosure. The Examiner, therefore, used impermissible hindsight in selecting the references and simply used Applicants' claims as guideposts to select the references even though the references are in dissimilar fields and have no motivation to combine with each other.

Conclusion

As a result of the foregoing, it is asserted by Applicants that the remaining claims in the Application are in condition for allowance, and Applicants respectfully request an early allowance of such claims.

Respectfully submitted,

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